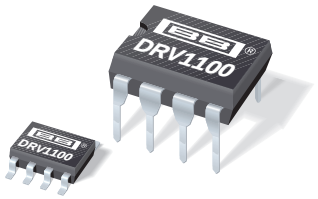
BURR-BROWN®



DRV1100

HIGH POWER DIFFERENTIAL DRIVER AMPLIFIER

FEATURES

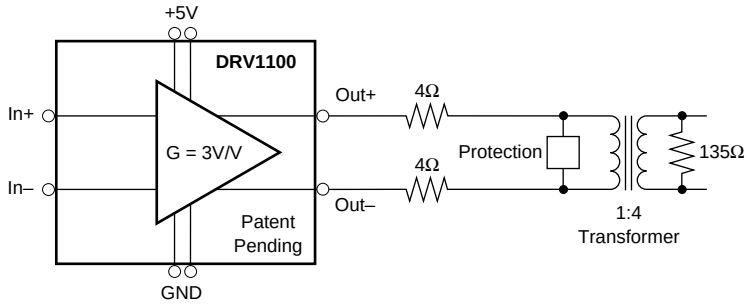
- **HIGH OUTPUT CURRENT: 230mA**
- **SINGLE SUPPLY OPERATION: 5V**
- **5MHz BANDWIDTH: 6Vp-p into 15Ω**
- **VERY LOW THD AT HIGH POWER: –72dBc at 6Vp-p, 100kHz, 100Ω**
- **LOW QUIESCENT CURRENT: 11mA**
- **FIXED DIFFERENTIAL GAIN: 3V/V**

APPLICATIONS

- **xDSL TWISTED PAIR LINE DRIVER**
- **COMMUNICATIONS LINE DRIVER**
- **TRANSFORMER DRIVER**
- **SOLENOID DRIVER**
- **HIGH POWER AUDIO DRIVER**
- **CRT YOKE DRIVER**

DESCRIPTION

The DRV1100 is fixed gain differential line driver designed for very low harmonic distortion at the high powers required of xDSL line interface standards. Operating on a single +5V supply, it can deliver 230mA peak output current and 9.5Vp-p differential output voltage swing. This high output power on a single +5V supply makes the DRV1100 an excellent choice for the xDSL applications that require up to 17dBm power onto the line with high crest factors. The DRV1100 is available in both 8-pin plastic DIP and SO-8 packages.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1354
Printed in U.S.A. December, 1996
SBWS004

SPECIFICATIONS

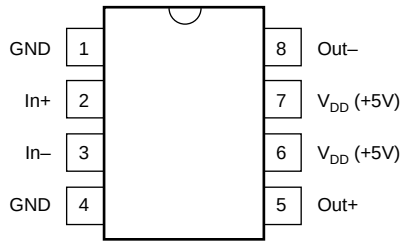
At V_{DD} = +5.0V, V_{CM} = V_{DD}/2, T_A = 25°C, unless otherwise specified.

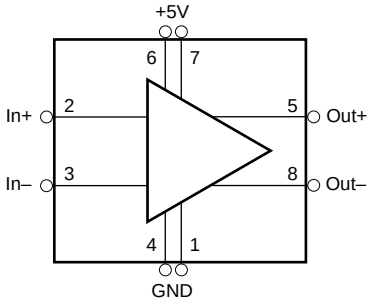
PARAMETER	CONDITIONS	DRV1100P, U			UNITS
		MIN	TYP	MAX	
AC PERFORMANCE					
–3dB Bandwidth	R_L = 15Ω, V_O = 1Vp-p		8		MHz
	R_L ≥ 100Ω, V_O = 1Vp-p		11		MHz
	R_L = 15Ω, V_O = 6Vp-p		5		MHz
	R_L ≥ 100Ω, V_O = 6Vp-p		6		MHz
Differential Slew Rate	R_L = 100Ω, V_O = 6Vp-p		80		V/µs
Step Response Delay[1]	V_O = 1Vp-p		25		ns
Settling Time to 1%, Step Input	V_O = 1Vp-p, R_L = 100Ω		0.25		µs
Settling Time to 1%, Step Input	V_O = 6Vp-p, R_L = 100Ω		0.3		µs
Settling Time to 0.1%, Step Input	V_O = 1Vp-p, R_L = 100Ω		0.8		µs
Settling Time to 0.1%, Step Input	V_O = 6Vp-p, R_L = 100Ω		1.1		µs
THD, Total Harmonic Distortion[2]					
f = 10kHz	R_L = 100Ω, V_O = 6Vp-p		–85		dBc
f = 10kHz	R_L = 15Ω, V_O = 6Vp-p	–66	–76		dBc
f = 100kHz	R_L = 100Ω, V_O = 6Vp-p		–72		dBc
f = 100kHz	R_L = 15Ω, V_O = 6Vp-p		–65		dBc
Input Voltage Noise	f = 100kHz		30		nV/√Hz
Input Current Noise	f = 100kHz		0.5		fA/√Hz
INPUT CHARACTERISTICS					
Differential Input Resistance			10^{11}		Ω
Differential Input Capacitance			1		pF
Common-Mode Input Resistance			10^{11}		Ω
Common-Mode Input Capacitance			6		pF
Input Offset Voltage			5		mV
Input Bias Current			1		pA
Common-Mode Rejection Ratio	Input Referred		62		dB
Power Supply Rejection Ratio	Input Referred	60	76		dB
Input Common-Mode Voltage Range[3]		0.5		V_{DD} –0.5	V
OUTPUT CHARACTERISTICS					
Differential Output Offset, RTO			10	25	mV
Differential Output Offset Drift, RTO	–40°C to +85°C		30		µV/°C
Differential Output Resistance			0.16		Ω
Peak Current (Continuous)	R_L = 15Ω	200	230		mA
Differential Output Voltage Swing	R_L = 1kΩ		9.6		Vp-p
	R_L = 100Ω	8.5	9.5		Vp-p
	R_L = 15Ω	6.0	6.6		Vp-p
Output Voltage Swing, Each Side	R_L = 1kΩ	0.125		4.875	V
Gain	Fixed Gain, Differential		3		V/V
Gain Error				±0.25	dB
POWER SUPPLY					
Operating Voltage Range		+4.5	+5.0	+5.5	V
Quiescent Current	V_{DD} = 5.0V		+11	+16	mA
TEMPERATURE RANGE		–40		+85	°C
Thermal Resistance, θ_{JA}					
DRV1100P 8-Pin DIP			100		°C/W
DRV1100U 8-Pin SO-8			125		°C/W

NOTES: (1) Time from 50% point of input step to 50% point of output step. (2) Measurement Bandwidth = 500kHz. (3) Output common-mode voltage follows input common-mode voltage; therefore, if input V_{CM} = V_{DD}/2, then output V_{CM} = V_{DD}/2.

PIN CONFIGURATIONS

Top View





ABSOLUTE MAXIMUM RATINGS

Analog Inputs: Current	±100mA, Momentary
	±10mA, Continuous
Voltage	GND –0.3V to V_{DD} +0.2V
Analog Outputs Short Circuit to Ground (+25°C)	Momentary
Analog Outputs Short Circuit to V_{DD} (+25°C)	Momentary
V_{DD} to GND	–0.3V to 6V
Junction Temperature	+150°C
Storage Temperature Range	–40°C to +125°C
Lead Temperature (soldering, 3s)	+260°C
Power Dissipation	(See Thermal/Analysis Discussion)

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
DRV1100P	8-Pin PDIP	006
DRV1100U	8-Lead SO-8	182

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

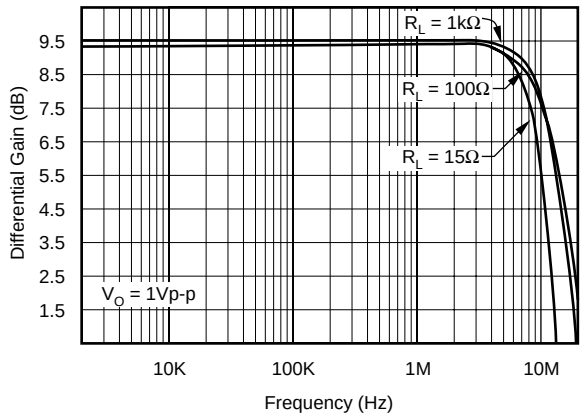
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

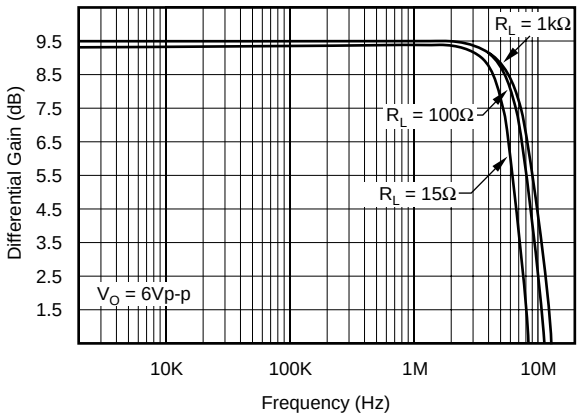
TYPICAL PERFORMANCE CURVES

At V_{DD} = +5.0V, V_{CM} = V_{DD}/2, T_A = 25°C, unless otherwise specified.

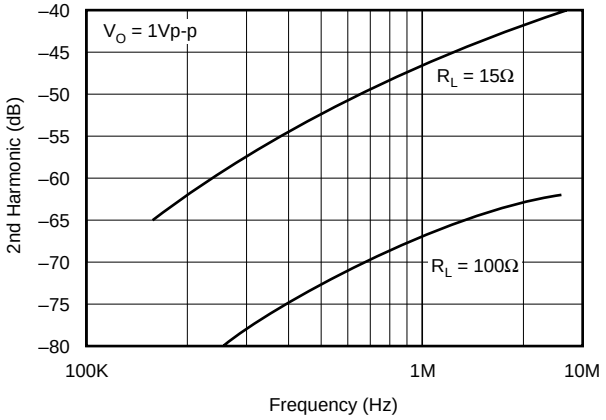
SMALL SIGNAL FREQUENCY RESPONSE



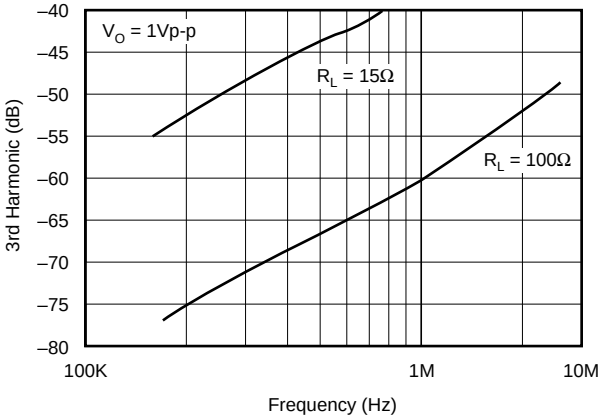
LARGE SIGNAL FREQUENCY RESPONSE



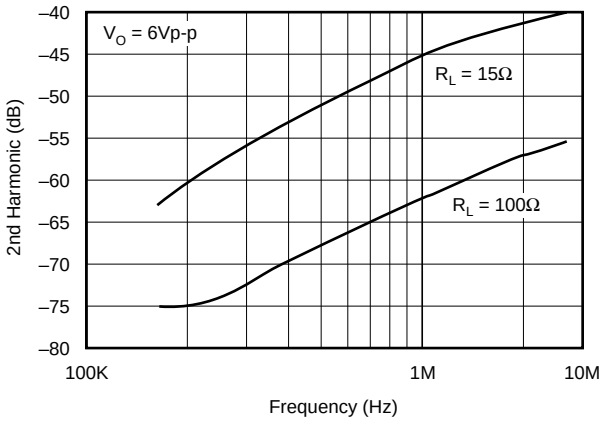
SMALL SIGNAL 2ND HARMONIC DISTORTION



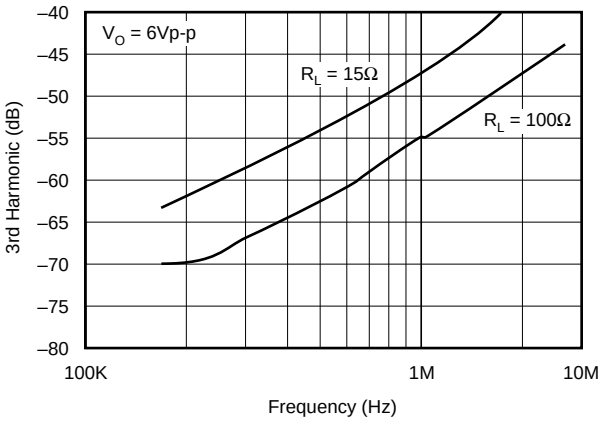
SMALL SIGNAL 3RD HARMONIC DISTORTION



LARGE SIGNAL 2ND HARMONIC DISTORTION

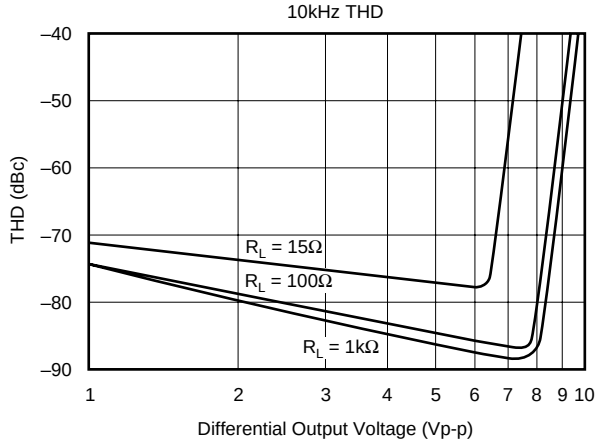


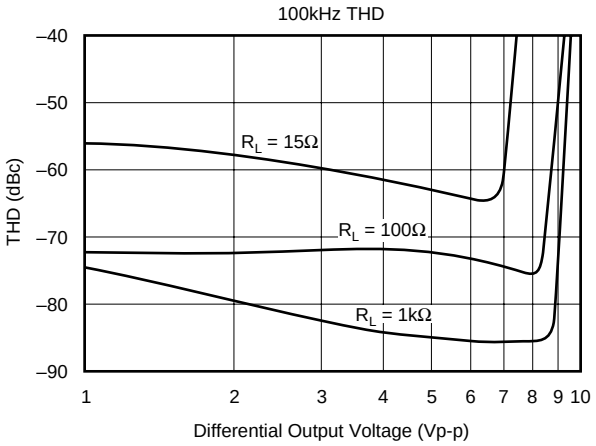
LARGE SIGNAL 3RD HARMONIC DISTORTION

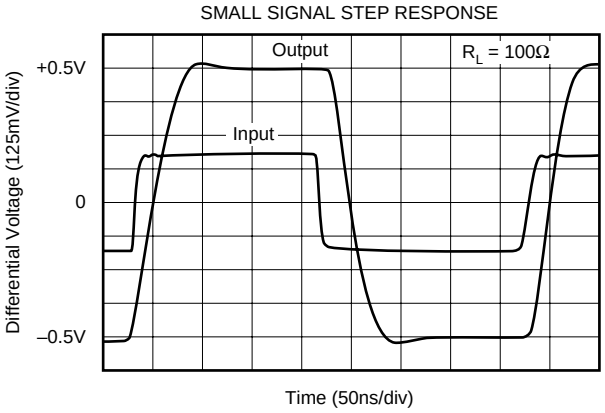


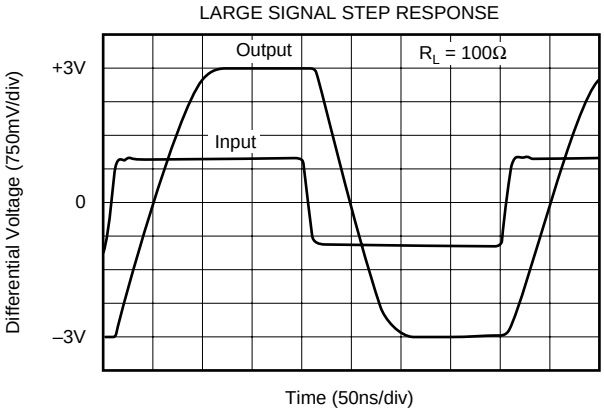
TYPICAL PERFORMANCE CURVES (CONT)

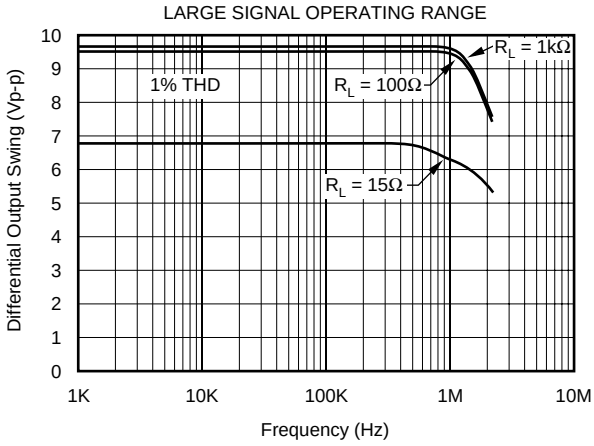
At V_{DD} = +5.0V, V_{CM} = V_{DD}/2, T_A = 25°C, unless otherwise specified.

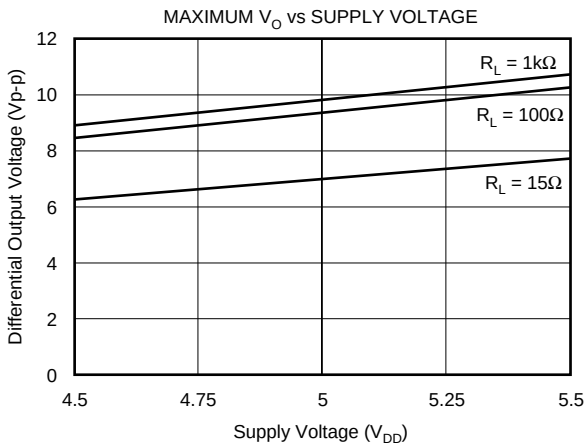








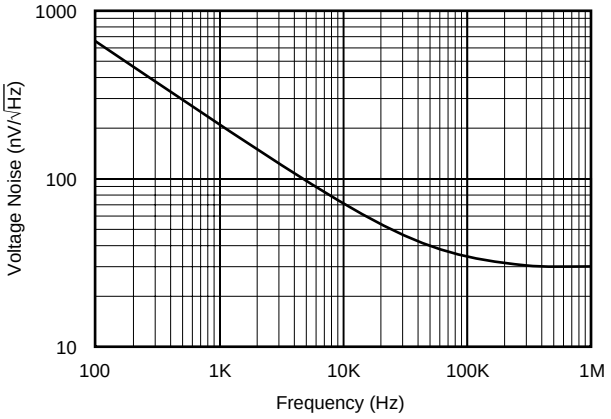




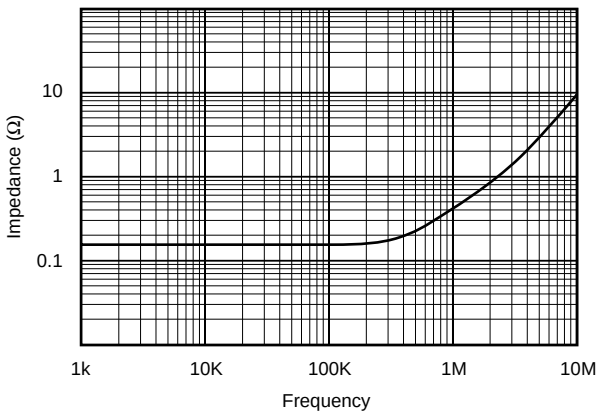
TYPICAL PERFORMANCE CURVES (CONT)

At V_{DD} = +5.0V, V_{CM} = V_{DD}/2, T_A = 25°C, unless otherwise specified.

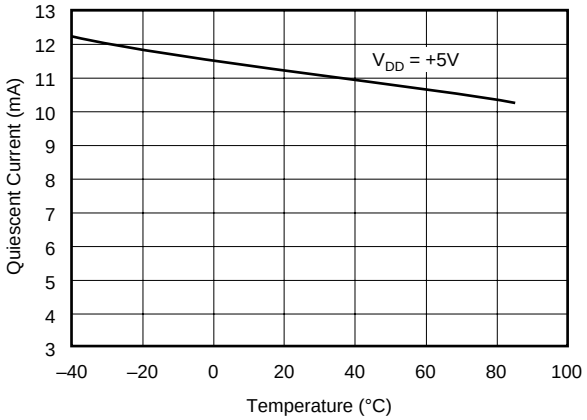
DIFFERENTIAL INPUT VOLTAGE NOISE



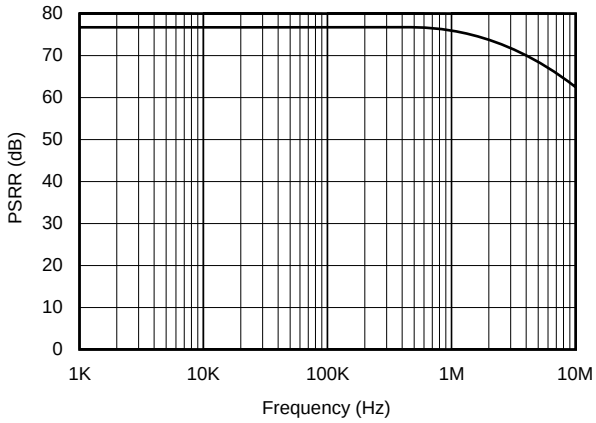
DIFFERENTIAL OUTPUT IMPEDANCE



QUIESCENT CURRENT vs TEMPERATURE



POWER SUPPLY REJECTION vs FREQUENCY



APPLICATIONS INFORMATION

INTERNAL BLOCK DIAGRAM

The DRV1100 is a true differential input to differential output fixed gain amplifier. Operating on a single +5V power supply, it provides an internally fixed differential gain of +3 and a common-mode gain of +1 from the input to output. Fabricated on an advanced CMOS process, it offers very high input impedance along with a low impedance 230mA output drive. Figure 1 shows a simplified internal block diagram.

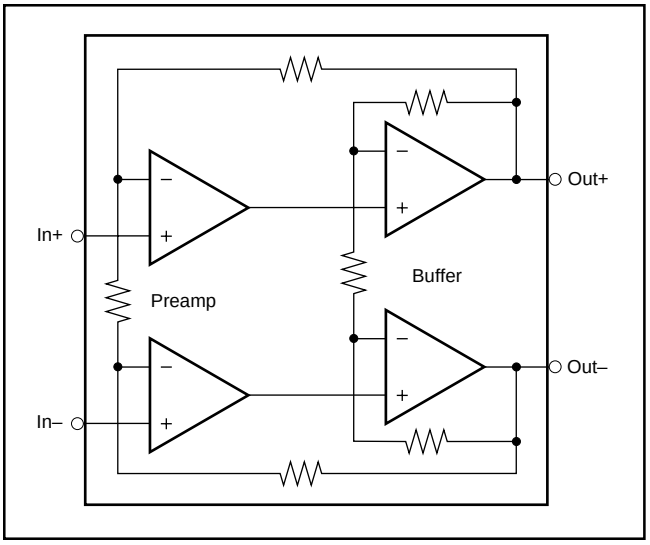


FIGURE 1. Simplified DRV1100 Internal Block Diagram.

To achieve the maximum dynamic range, operate the DRV1100 with the inputs centered at $V_{DD}/2$. This will place the output differential swing centered at $V_{DD}/2$ for maximum swing and lowest distortion. Purely differential input signals will produce a purely differential output signal. A single ended input signal, applied to one input of the DRV1100, with the other input at a fixed voltage, will produce both a differential and common-mode output signal. This is an acceptable mode of operation when the DRV1100 is driving an element with good common-mode rejection (such as a transformer).

DIFFERENTIAL OUTPUT VOLTAGE AND POWER

Applying the balanced differential output voltage of the DRV1100 to a load between the outputs will produce a peak-to-peak voltage swing that is twice the swing of each individual output. This is illustrated in Figure 2 where the common-mode voltage is $V_{DD}/2$. For a load connected between the outputs, the only voltage that matters is the differential voltage between the two outputs—the common-mode voltage does not produce any load current in this case.

The peak power that the DRV1100 can deliver into a differential load is V_P^2/R_L. The Typical Performance Curves show the maximum Vp-p versus load and frequency. The peak voltage (Vp) equals 1/2 of the peak-to-peak voltage

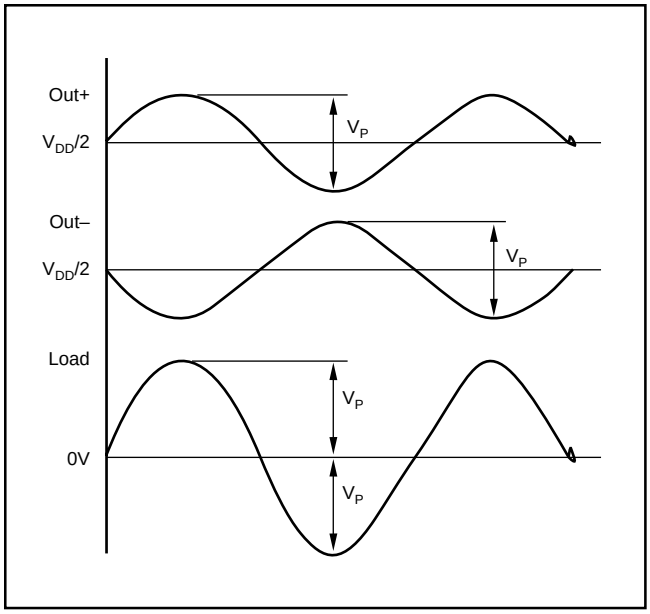


FIGURE 2. DRV1100 Single Ended and Differential Output Waveforms.

(Vp-p). Squaring 1/2 of the Vp-p and dividing by the load will give the peak power. For example, the Typical Performance Curves show that on +5V supply the DRV1100 will deliver 6.8Vp-p into 15Ω at 500kHz. The peak load power under this condition is $(6.8Vp\text{-}p/2)^2/15\Omega = 770mW$.

SUPPLY VOLTAGE

The DRV1100 is designed for operation on a single +5V supply. For loads > 200Ω, each output will swing rail to rail. This gives a peak-to-peak differential output swing that is approximately = 2 • V_{DD}. For best distortion performance, the power supply should be decoupled to a good ground plane immediately adjacent to the package with a 0.1µF capacitor. In addition, a larger electolytic supply decoupling capacitor (6.8µF) should be near the package but can be shared among multiple devices.

DIGITAL SUBSCRIBER LINE APPLICATIONS

The DRV1100 is particularly suited to the high power, low distortion, requirements of a twisted pair driver in digital communications applications. These include HDSL (High bit rate Digital Subscriber Lines), ADSL (Asymmetrical Digital Subscriber Lines), and RADSL (Rate adaptive ADSL). Figure 3 shows a typical transformer coupled xDSL line driver configuration. In general, the DRV1100 is usable for output power requirements up to 17dBm with a crest factor up to 6 (crest factor is the ratio of peak to rms voltage).

To calculate the required amplifier power for an xDSL application—

- Determine the average power required onto the line in the particular application. The DRV1100 must be able to deliver twice this power (+3dB) to account for the power

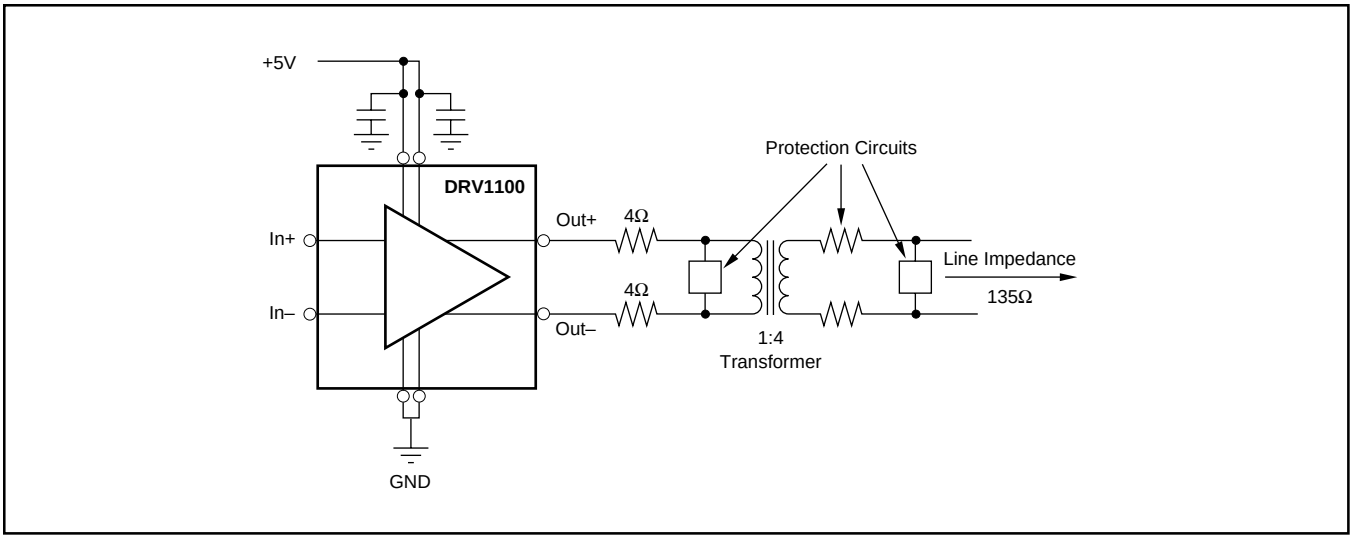


FIGURE 3. Typical Digital Subscriber Line Application.

loss through the series impedance matching resistors shown in Figure 3. **Twice the required line power must be delivered by the DRV1100 through the frequency band of interest with the distortion required by the system.**

- Calculate the RMS voltage required at the output of the DRV1100 with this 2X line power requirement. Vrms = $(2 \cdot P_{LINE} \cdot R_L)^{1/2}$, where R_L is the total load impedance that the DRV1100 must drive. Multiply this Vrms by 2 • crest factor to get the total required differential peak-to-peak voltage at the output. **The DRV1100 must be able to drive the peak-to-peak differential voltage into the load impedance.**

Where possible, the transformer turns ratio may be adjusted to keep within the DRV1100 output voltage and current constraints for a given R_{LINE} and desired power onto the line.

Using the example of Figure 3, assume the average power desired on a 135Ω line is 14dBm (HDSL). Twice this power (17dBm) is required into the matching resistors on the primary side of the transformer. This 135Ω load is reflected through the 1:4 transformer as a $(135/(4^2)) = 8.4\Omega$ load. The two series 4.1Ω resistors, along with the 0.2Ω differential output impedance of the DRV1100, will provide impedance matching into this 8.4Ω load. The DRV1100 will see approximately a 16.5Ω load under these conditions. The required 17dBm (50mW) into this load will need an output Vrms = $(50mW \cdot 16.5)^{1/2}$ = 0.91Vrms. Assuming a crest factor of 3, the differential peak-to-peak output voltage = 6 • 0.91 = 5.45Vp-p. The Typical Performance Curves show that, at 100kHz, the DRV1100 can deliver this voltage swing with less than –62dB THD.

OUTPUT PROTECTION

Figure 3 also shows overvoltage and short circuit protection elements that are commonly included in xDSL applications. Overvoltage suppressors include diodes or MOV's. The outputs of the DRV1100 can be momentarily shorted to ground or to the supply without damage. The outputs are not, however, designed for a continuous short to ground or the supply.

POWER DISSIPATION AND THERMAL ANALYSIS

The total internal power dissipation of the DRV1100 is the sum of a quiescent term and the power dissipated internally to deliver the load power. The Typical Performance Curves show the quiescent current over temperature. At +5V supply, the typical no load supply current of 11mA will dissipate 55mW quiescent power. The rms power dissipated in the output circuit to deliver a Vrms to a load R_L is:

$$Prms = (V_{DD} - Vrms) \cdot (Vrms/R_L)$$

The internal power dissipation will reach a maximum when Vrms is equal to $V_{DD}/2$. For a sinusoidal output, this corresponds to an output Vp-p = 1.41 • V_{DD}.

As an example, compute the power and junction temperature under a worst case condition with V_{DD} = +5V and Vrms = 2.5V into a 16Ω differential load (peak output current for a sinusoid would be 222mA). The total internal power dissipation would be:

$$(5V \cdot 11mA) + (5V - 2.5V) \cdot (2.5V/16\Omega) = 446mW$$

To compute the internal junctions temperature, this power is multiplied by the junction to ambient thermal impedance (to get the temperature rise above ambient) then added to the ambient temperature. Using the specified maximum ambient temperature of +85°C, the junction temperature for the DRV1100 in an SO-8 package under these worst case conditions will be:

$$T_J = 85°C + 0.446W \cdot 125°C/W = 141°C$$

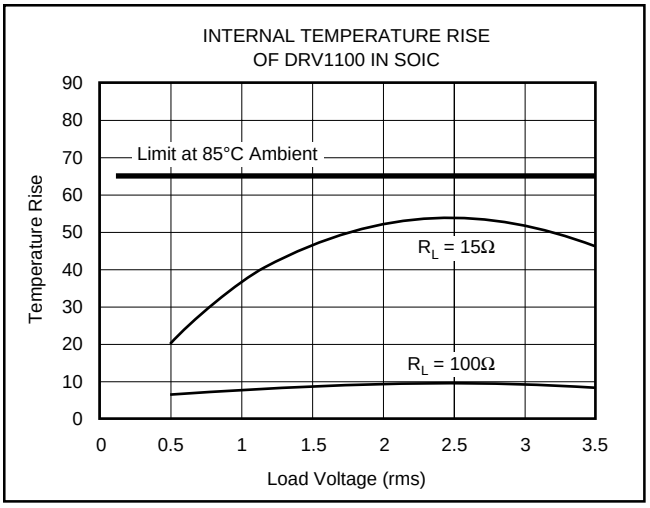


FIGURE 4. Junction Temperature Rise From Ambient for the DRV1100U.

The internal junction temperature should, in all cases, be limited to < 150°C. For a maximum ambient temperature of +85°C, this limits the internal temperature rise to less than 65°C. Figure 4 shows the temperature rise from ambient to junction for loads of 15Ω and 100Ω. This shows that the internal junction temperature will never exceed the rated maximum for a 15Ω load.

INPUT INTERFACE CIRCUITS

Best performance with the DRV1100 is achieved with a differential input centered at $V_{DD}/2$. Signals that do not require DC coupling may be connected as shown in Figure 5 through blocking caps to a midpoint reference developed through resistor dividers from the supply voltage. The value for the R_B resistors determine four performance requirements.

- They bias the inputs at the supply midpoint.
- They provide a DC bias current path for the input to the DRV1100
- They set the AC input impedance for the source signals to $R_B/2$.
- They set the low frequency cutoff frequency along with C_B.

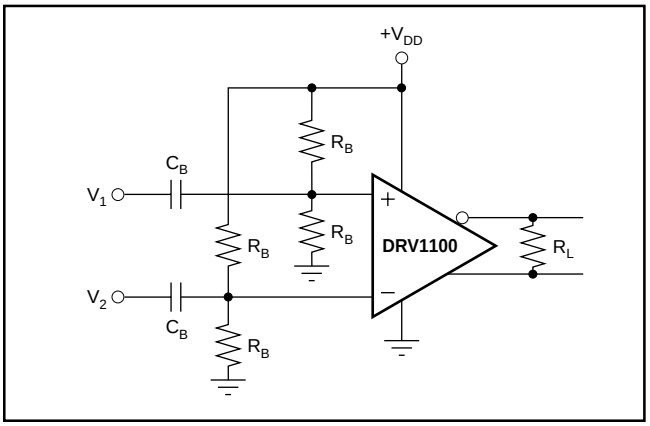


FIGURE 5. AC Coupled Differential Input Interface.

Often, the R_B resistors will be set to a relatively high value (> 10kΩ) to minimize quiescent current in the reference path. If a lower input impedance is desired, additional terminating resistors may be added to the input side of the blocking capacitors (C_B).

The circuit of Figure 5 may also be operated with only a single ended input. In that case, the reference voltage on the other input should be decoupled to ground with a 0.1µF capacitor. In this connection, the input will generate unbalanced outputs. The differential output voltage will still be 3 times the input peak-to-peak voltage, but since there is now a common-mode voltage input, there will be a common mode voltage output. The output common-mode voltage will be equal to the input signal's peak-to-peak swing. This common-mode component will reduce the available differential output voltage swing. However, if the output load has good common-mode rejection, such as a transformer, this is an acceptable way of using the DRV1100 with a single ended source.

Figure 6 shows a means of translating a ground centered single ended input to a purely differential signal for application to DRV1100 input. This circuit uses a wideband dual op amp in cross coupled feedback configuration.

The outputs of this circuit may then be fed into the inputs of Figure 5. The total gain of Figure 6 is $2 \cdot (R_F/R_G)$. The circuit will act to hold all 4 op amp inputs equal to the + input of the lower op amp. Since this is at ground, the midpoint for the input signal (where the two outputs will be equal) is also at 0V.

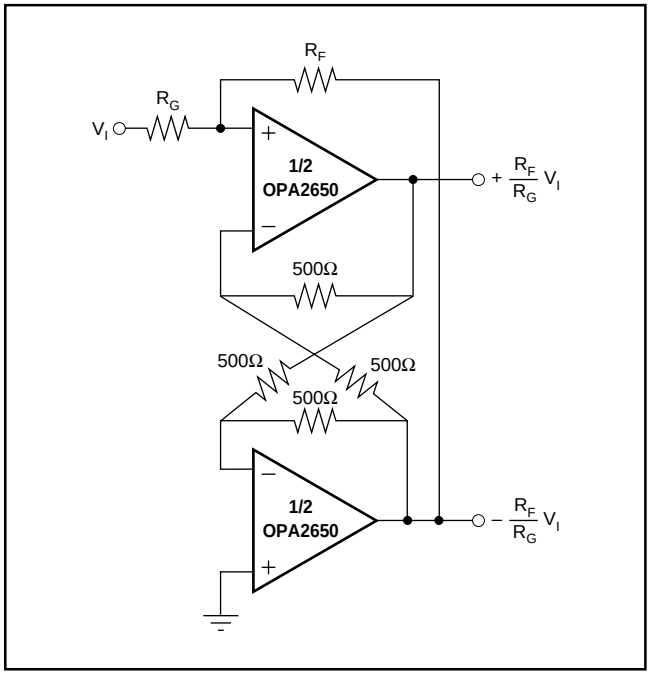


FIGURE 6. Single Ended to Differential Conversion.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DRV1100U	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DRV1100U/2K5	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DRV1100U/2K5G4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
DRV1100UG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

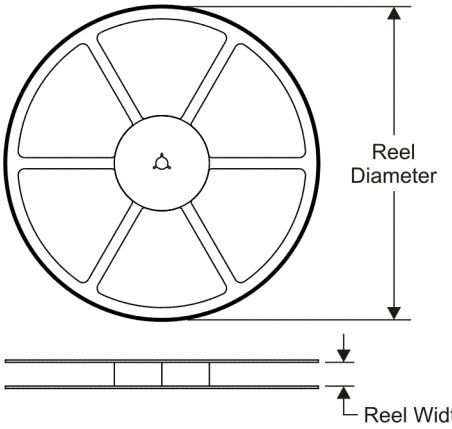
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

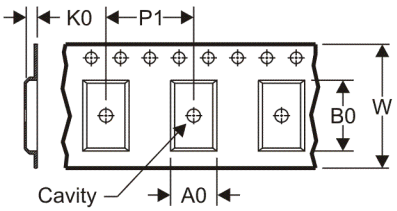
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

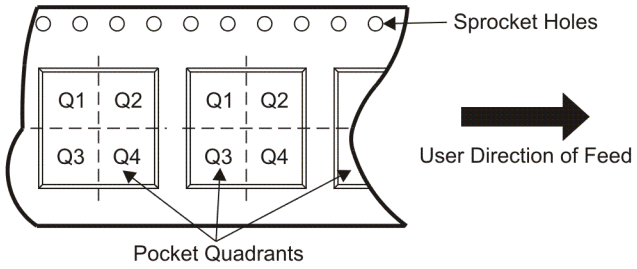


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

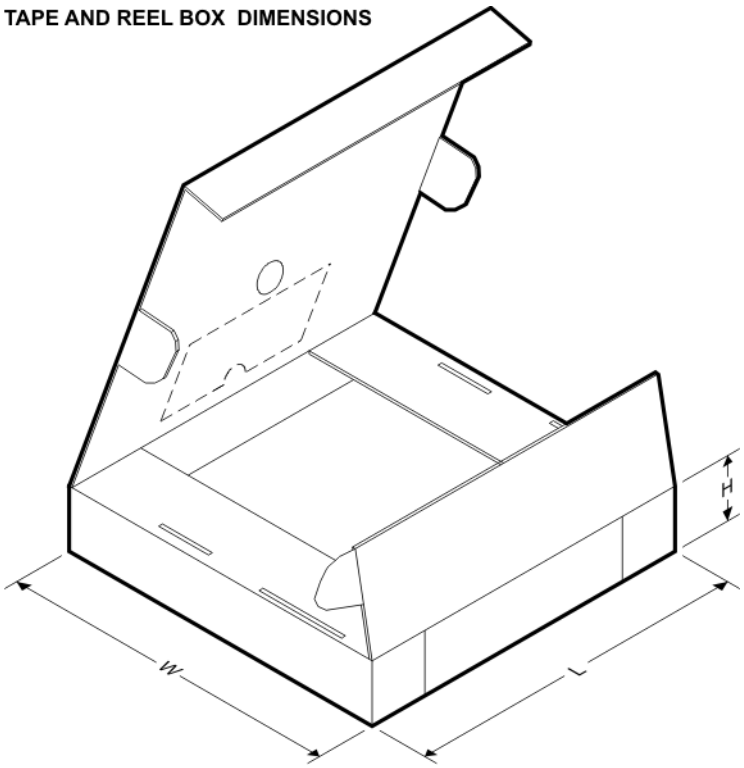
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV1100U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV1100U/2K5	SOIC	D	8	2500	346.0	346.0	29.0

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